PERGAMON

Neural Networks 12 (1999) 211–216

Neural Networks

Neural Networks Letter

A subthreshold MOS circuit for the Lotka–Volterra neural network producing the winners-share-all solution

T. Asai[a,*], T. Fukai[b,c], S. Tanaka[c]

[a]*Department of Electrical and Electronic Engineering, Toyohashi University of Technology, Hibarigaoka 1-1, Tempaku-cho, Toyohashi, Aichi, 441-8580, Japan*

[b]*Department of Electronics, Tokai University, Kitakaname 1117, Hiratsuka, Kanagawa, 259-1207, Japan*

[c]*Laboratory for Neural Modeling, Brain Science Institute, The Institute of Physical and Chemical Research (RIKEN), 2-1, Hirosawa, Wako, Saitama 351-0198, Japan*

Received 22 July 1998; received in revised form 9 September 1998; accepted 9 September 1998

Abstract

An analog MOS circuit is proposed for implementing a Lotka–Volterra (LV) competitive neural network which produces winners-share-all solutions. The solutions give multiple winners receiving large inputs and are particularly useful for selecting a set of inputs through ''decision by majority''. We show that the LV network can easily be implemented using subthreshold MOS transistors. Results of extensive circuit simulations prove that the proposed circuit does exhibit a reliable selection compared with winner-take-all circuits, in the possible presence of device mismatches. These results pave a way to future implementation on a real device.

1. Introduction

The winner-take-all (WTA) competition provides a way to select the input of upmost importance (Cohen & Grossberg, 1983; Majani et al., 1989, 1989; Yuille, 1989; Wolfe et al., 1991; Kaski & Kohonen, 1994; Taylor & Alavi, 1995). The result of competition is typically represented by the activation of a single neuron which receives the largest input. The WTA competition, however, does not suit for an analog circuit implementation since the selection of a single winner may easily suffer from noise in inputs, partial destructions of the circuits or deviations in physical parameters of a group of equally designed devices (Lakshmikumar et al., 1986; Pelgrom et al., 1989).

A Lotka–Volterra (LV) neural network, which was recently derived from the membrane dynamics of competing neurons, possesses three types of steady-state solutions (Fukai & Tanaka, 1997). Those solutions are classified as the WTA, winners-share-all (WSA) and variant winner-take-all (VWTA). The WSA solution gives multiple winners in the order of magnitudes of external inputs. The number of winners can easily be adjusted by a single parameter in the model. The selection of winners for WTA and WSA cases does not depend on initial values of neuron variables, whereas that for VWTA case does.

Among those solutions, the WSA solution can be used to reduce the influence of the noise and device mismatches of the analog circuits if an external signal is selected by multiple winners. In this letter, we propose a MOS circuit producing the WSA solution of the LV networks for exploring a possible solution to the difficulties in the matching analog devices. Since the MOS transistors in the proposed circuit operate in a subthreshold region, the electric power dissipation from the circuit is very small. The low power dissipation is critical for realizing a large scale circuit. In order to examine the influences of device mismatches on the circuit's performance, we conduct extensive simulations of the proposed LV circuit with Simulation Program of Integrated Circuit Emphasis (SPICE). The implementation on a real device is reported elsewhere (Asai et al., 1997).

2. The Lotka–Volterra competitive neural network

The LV equation which describes competitive behavior among N identical neurons is given as (Fukai & Tanaka,

* Corresponding author; e-mail: asai@postone.com

0893-6080/99/$ - see front matter
PII: S0893-6080(98)00121-X

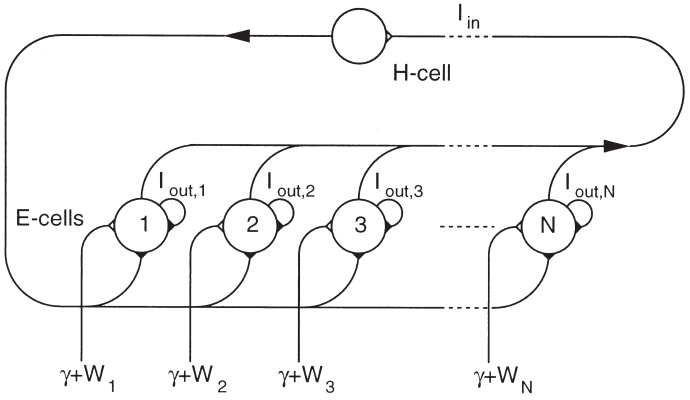

Fig. 1. The circuit for the LV neural network with N external inputs. The circuit consists of a single inhibitory neuron unit (H-Cell) and N excitatory neuron units (E-cells).

1997)

$$\tau\frac{\mathrm{d}z_i}{\mathrm{d}t} = z_i\left(\gamma + W_i - z_i - \lambda\sum_{j\neq i} z_j\right) + \varepsilon, \qquad i = 1,\ldots,N \tag{1}$$

where z_i is the activity of the ith neuron, γ represents an input which is nonspecific to each neuron, W_i represents neuron-dependent inputs and ϵ is a small positive constant. The ϵ term prevents any z_i from becoming 0, so that losers and winners can interchange if the magnitudes of $\{W_i\}$ are changed occasionally. Each neuron has a self-inhibitory connection of the strength normalized to unity and λ is the relative strength of all-to-all lateral inhibitory connections.

Let the external inputs obey

$$W_1 \geq W_2 \geq W_3 \geq \cdots \geq W_{N-1} \geq W_N \geq 0, \tag{2}$$

and $\epsilon = 0$ for the time being. The WSA solution to the LV equation appears when

$$\lambda < \lambda_- \equiv \frac{\gamma + W_1}{\gamma + 2W_1 - W_2}. \tag{3}$$

The winners are neurons which receive d largest external inputs among all. The steady-state solution with d winners is given by

$$\begin{aligned} z_i &= \frac{1}{\alpha} + \frac{W_i}{1-\lambda} + \frac{\lambda d}{(\lambda-1)\alpha}\langle W\rangle_D, \qquad i = 1,\ldots,d \\ z_i &= O(\varepsilon), \qquad i = d+1,\ldots,N \end{aligned} \tag{4}$$

independently of initial values of z_i, where $\alpha \equiv d\lambda + 1 - \lambda, \langle W\rangle_D \equiv d^{-1}\sum_{j=1}^{d} W_j$. The actual number of winners can be determined implicitly by

$$\gamma + W_d > \frac{\lambda d}{1-\lambda}(\langle W\rangle_D - W_d). \tag{5}$$

The r.h.s. of (5) is an increasing function of d while the l.h.s. is a decreasing function of d. Thus there exists an upper bound for d above which condition (5) is not satisfied. This upper bound gives the number of winners.

Condition(5) indicates that the number of winners decreases, and finally becomes one, as the relative strength λ of the lateral inhibition approaches unity. On the other hand, all the neurons remain active for λ less than $\lambda_L \equiv (\gamma + W_N)/\left(\gamma + W_N + \sum_{j=1}^{N} W_j - NW_N\right)$, which means that no neural selection occurs for $0 < \lambda < \lambda_L$. Note that $0 < \lambda_L < \lambda_- < 1$.

The WTA $(\lambda_- < \lambda < \lambda_+ \equiv (\gamma + W_1)/(\gamma + W_2))$ and VWTA $(\lambda > \lambda)$ solutions to the LV equation were also obtained by Fukai & Tanaka (1997), but they are not discussed here since we consider those solutions less important in the circuit than the WSA solutions.

3. An analog circuit for the Lotka–Volterra neural network

The LV equation can be transformed into a form more suitable for analog circuit implementation.

Introducing new variables $y_i = \ln z_i$, we can rewrite (1) as

$$\tau\dot{y}_i = \gamma' + W_i - \exp(y_i) - \lambda\sum_{j\neq i}^{N}\exp(y_i). \tag{6}$$

where γ' represents $\gamma + \varepsilon\exp(-y_i)$. The circuit implementation of the system described by (6) is much easier than that of (1), because (i) the products of the system variables disappear, and (ii) each processing unit has an exponential response function, a fundamental characteristics of many types of semiconductor device. Although the present LV neural network has all-to-all connections, the complexity of the connections can be easily reduced to O(N) owing the uniformity in the strength of lateral inhibition. Namely, we rewrite (6) as

$$\tau\dot{y}_i = \gamma + W_i - (1-\lambda)\exp(y_i) - \lambda\sum_{j=1}^{N}\exp(y_i), \tag{7}$$

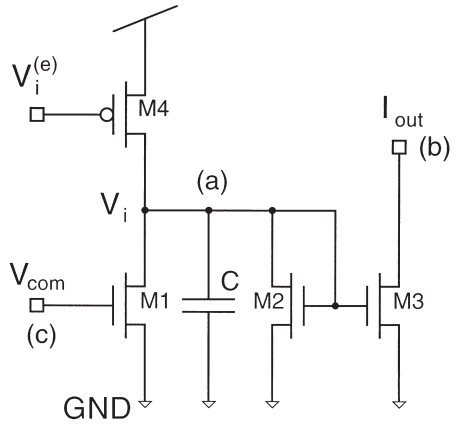

Fig. 2. The E-cell circuit composed of four MOS transistors. Each external input is given to the circuit as the gate voltage $V_i^{(e)}$. The E-cell circuits are connected with the H-cell circuit through the terminals (b) and (c).

and introduce N excitatory cells (E cells) and one inhibitory cell (H cell) as shown in Fig. 1. Note that the ϵ-dependent term in γ' is omitted since the term is not necessary in the circuit implementation of (6) because of a property of MOS transistors, as will be seen later. The H cell receives an excitatory connection of unit strength from each E cell, while an E cell receives an afferent input $\gamma + W_i$, a self-inhibitory connection of strength $(1 - \lambda)$ and an inhibitory connection of strength λ from the H cell. The response functions of the E cell and H cell are defined as $\exp(x)$ and x, respectively. We use this system for the circuit implementation of our LV neural network. In this way, a large-scale neural network could be implemented on a small chip area owing to the simple circuit structure of neuron units and O(N) complexity of connections among the units.

Figs. 2 and 3 show schematic diagrams of the E- and H-cell circuits realized by a small number of MOS transistors,

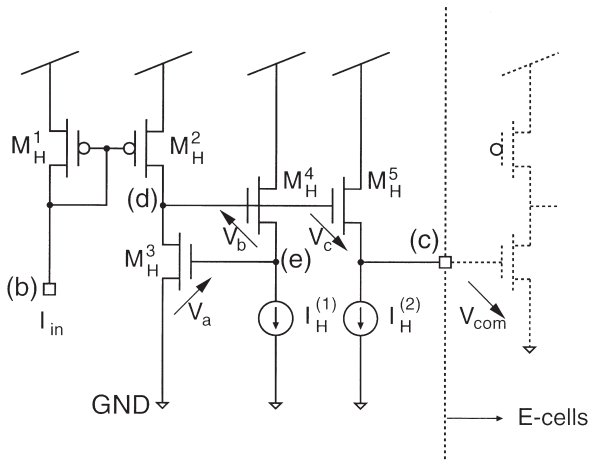

Fig. 3. The H-cell circuit composed of five MOS transistors. The parameter λ of the LV neural network is controlled by the current source magnitude ratio $(I_H^{(1)}/I_H^{(2)})$.

respectively. Applying Kirchhoff's current law (KCL) at node (a) in Fig. 2, we can obtain the equation

$$C\dot{V}_i = I_i^{M_4} - I_i^{M_1} - I_i^{M_2}, \tag{8}$$

where C and I_i^{Ma} stand for a MOS capacitance and the current of transistor M_i^a of the ith E-cell circuit. In the subthreshold region of operation, $I_i^{M_2}$ is ideally given by

$$I_i^{M_2} = I_0 \exp(kV_i/V_T), \tag{9}$$

where I_0 is the zero-bias current for the given device, $V_T = kT/q$ (k is the Boltzmann constant, T is temperature and q is the charge of an electron), and k measures the effectiveness of the gate potential. Similarly, $I_i^{M_1}$ is given as

$$I_i^{M_1} = I_0 \exp(kV_{com}/V_T) \tag{10}$$

in terms of the gate-source voltage of transistor M_i^1, as long as it operates in the saturation region $(V_i \geq 4V_T)$. The current mirror structure of M_i^2 and M_i^3 implies that $I_i^{M_3}$ or the output current of the ith circuit is equal to $I_i^{M_2}$. Applying KCL at common node (b), we obtain the current $I_H^{M_1}$ of M_H^1 in the H-cell circuit as

$$I_H^{M_1} = I_0 \sum_{j=1}^{N} \exp(kV_j/V_T), \tag{11}$$

which is equal to $I_H^{M_2}$ of the current mirror structure. The current $I_i^{M_2}$ which represents the global inhibition on E cells needs to be mirrored to $I_i^{M_1}$ with an externally modifiable ratio. To this end, the transistors M_H^3, M_H^4, M_H^5 in the H-cell circuit and $M_i^1 (i = 1, 2 \ldots N)$ in the E-cell circuits are employed as translinear multiplier/divider (Andreou et al., 1991). Then summing the voltages around the loop GND–(e)–(d)–(c)–GND in Fig. 3 imposes the following relation on the voltages in the H-cell circuit:

$$V_a + V_b + V_c + V_{com} = 0, \tag{12}$$

where V_a, V_b and V_c stand for the gate-source voltages of transistors M_H^3, M_H^4 and M_H^5, respectively. Representing the gate-source voltages with their respective drain-source subthreshold currents, and assuming that all devices have identical values for k and I_0, we obtain

$$\frac{V_T}{k}\ln\left(\frac{I_H^{M_1}}{I_0}\right) + \frac{V_T}{k}\ln\left(\frac{I_H^{(1)}}{I_0}\right) - \frac{V_T}{k}\ln\left(\frac{I_H^{(2)}}{I_0}\right) - \frac{V_T}{k}\ln\left(\frac{I_i^{M_1}}{I_0}\right) = 0 \tag{13}$$

From (11) and (13), we can easily derive

$$I_i^{M_1} = \frac{I_H^{(1)} I_H^{M_1}}{I_H^{(2)}} = \beta I_0 \sum_{j=1}^{N} \exp(kV_j/V_T), \tag{14}$$

where β represents the ratio of $I_H^{(1)}$ to $I_H^{(2)}$. By replacing

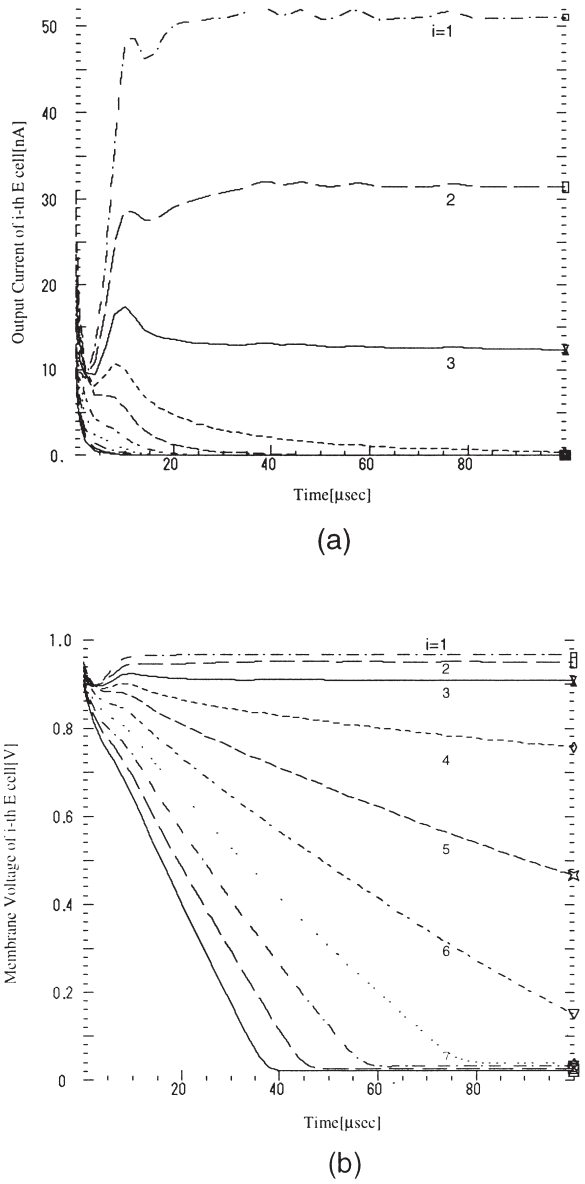

Fig. 4. The dynamic behavior of the circuit model showing the WSA solution with three winners. The time courses of the output currents $I_i^{M_2}$ and the membrane voltages V_I at the node of the E cells are presented in (a) and (b), respectively.

the current sources for $I_H^{(1)}$ and $I_H^{(2)}$ with MOS transistors operating in the saturation region, β is rendered externally modifiable through the gate voltages of those transistors.

The afferent input to each E cell is given by an input current to transistor M_i^4. Therefore, the strength of the afferent input can be externally controlled by changing the gate voltage $V_i^{(e)}$ of M_i^4 through

$$I_i^{M_4} = I_0 \exp(-kV_i^{(e)}/V_T). \tag{15}$$

Here $V_i^{(e)}(< 0)$ must be in the range which ensures the operation of M_i^4 in the subthreshold region.

Now substituting (9), (14) and (15) into (8), we obtain

$$C\dot{V}_i = I_0 \exp(-kV_i^{(e)}/V_T) - I_0 \exp(kV_i/V_T) - \beta I_0 \sum_{j=1}^{N} \exp(kV_j/V_T), \tag{16}$$

which becomes equivalent to (6) with the following substitution:

$$\frac{CV_T}{I_0 k(1+\beta)} \equiv \tau, \qquad \frac{k}{V_T} V_i \equiv y_i, \qquad \frac{\exp(-kV_i^{(e)}/V_T)}{1+\beta} \equiv \gamma' + W_i, \qquad \frac{\beta}{1+\beta} \equiv \lambda. \tag{17}$$

Note that λ is in the interval (0,1) since $\beta > 0$. Therefore, the proposed circuit produces WSA solutions as required.

In practice we can omit the ϵ-term in the circuit implementation and simply replace γ' with γ in (17). The reason why this term can be omitted is as follows. Remember that the term was necessary in (1) to prevent z_i from becoming zero. Suppose that the LV neural network gives the WTA solution with cell 1 being a winner: $z_1 > 0$ and $z_i = 0$ for $i \neq 1$. In the transformed system (7), this means that $y_1 = \ln((\gamma' + W_1)/k)$ and all other y_i's are $-\infty$ because of the logarithmic relation $y_i = \ln z_i$. Large negative y_i for the losers implies that the inhibitory effects of the losers on the winner vanish and the effects of the winner on the losers dominate to give the WTA solution.

This divergence to negative infinity, however, never occurs in the circuit. When $V_i \leq 4V_T$ and M_i^1 starts to leave the saturation region, the relation (10) ceases to be valid. Consequently, the lateral inhibition term represented by $\beta I_0 \sum_{j=1}^{N} \exp(kV_j/V_T)$ in (16) decreases rapidly to zero, rather than to I_0, as V_I approaches zero in the equation for the losers. This indicates that V_i does not go to negative infinity for the losers because the driving term itself vanishes. Thus the losers acquire a small nonvanishing V_i, giving $z_i > 0$.

4. Simulation results

In the following SPICE simulations, the capacitance of the E cells and the dimensions of the MOS transistors are assumed as C=10 pF and W/L=6 μm/4 μm. For other parameters of the transistors, we employ the typical values provided by MOSIS (CMOS process, feature size: 2 μm).

A transient response of the WSA circuit with $N = 10$ is shown in Fig. 4. In this simulation, all transistors have identical values for the device parameters. Figs. 4(a) and (b) show the time courses of output currents $\{I_i^{M_2}\}$ and membrane voltages $\{V_i\}$ for $\lambda = 0.7$, which correspond to z_i and y_i respectively. The value of the afferent input current for each neural circuit is given by

$$I_i^{M_4} = 300 - 20 \times i \quad \text{(nA)}, \qquad i = 1, \ldots, 10. \tag{18}$$

The inequality (5) predicts that winners should be the

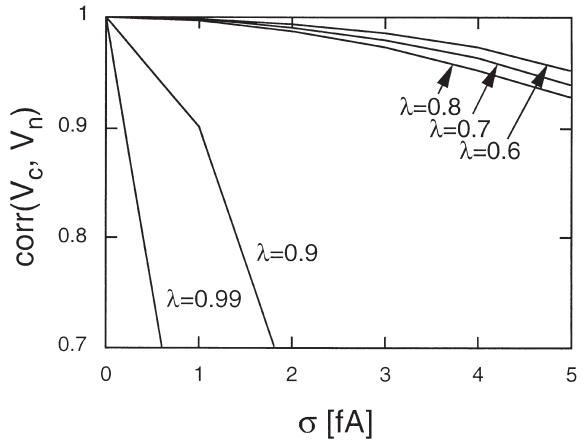

Fig. 5. Correlation between equilibrium voltages of the LV circuits with and without device mismatches as functions of a standard deviation of the mismatches.

neurouns receiving the first three largest inputs. The result shown in Fig. 4(a) is consistent with this prediction. From Fig. 4(b), it is also found that V_i for losers do not diverge to negative infinity, as expected.

Device mismatches of on-chip transistors are considered to be a drawback when we use the subthreshold regions. In the following simulations, the mismatches are embedded in the values of zero-bias current I_0 since they may vary for different transistors to a much greater extent than the values of k (Pavasovic et al., 1994). The following Gaussian distribution is assumed for I_0:

$$P(I_0) = \frac{1}{\sqrt{2\pi}\sigma}\exp\left(\frac{(I_0 - I_{\mathrm{av}})^2}{2\sigma^2}\right), \tag{19}$$

where I_{av} and σ represent the average value of the zero-bias currents and the standard deviation of I_0 respectively. I_{av} is fixed at 16 fA. The mismatches of I_0 will give rise to the deviations of the strength of lateral inhibition, and the inhomogeneous strength of lateral inhibition can result in erroneous selection of winners. We are interested in studying to what extent the WSA solution produced by the LV circuit is influenced by the magnitude of σ. The network performance is measured by the correlation function:

$$\mathrm{corr}(\boldsymbol{V}_c, \boldsymbol{V}_n) = \frac{\langle \boldsymbol{V}_c \cdot \boldsymbol{V}_n\rangle - \langle \boldsymbol{V}_c\rangle\langle \boldsymbol{V}_n\rangle}{\sqrt{\langle \boldsymbol{V}_c^2\rangle - \langle \boldsymbol{V}_c\rangle^2}\sqrt{\langle \boldsymbol{V}_n^2\rangle - \langle \boldsymbol{V}_n\rangle^2}} \tag{20}$$

where $\boldsymbol{V}_c$ represents the vector of equilibrium voltages V_i's in the LV circuit in the absence of the mismatches, while $\boldsymbol{V}_n$ represents the vector of the voltages in the presence of the mismatches. If the value of the correlation is close to unity, the influence of the device mismatches is small. The value of the afferent input current for each neural circuit is given by

$$I_i^{M_4} = i \quad (nA), \qquad i = 1, \ldots, 100. \tag{21}$$

Fig. 5 shows the results of simulations for LV circuit with N=100. The figure indicates that when the LV circuit produces a WTA solution ($\lambda \rightarrow 1$), even a small σ makes the selection of a solution unpredictable since an inappropriate neuron accidentally becomes a winner because of the mismatches. On the other hand, the selection becomes reliable as the number of winners is increased in the WSA solution ($\lambda < 0.9$). In the cases, correct winners are activated with high probability according to ''decision by majority''.

In actual analog VLSIs, the I_0 values of two nominally identical transistors may maximally differ by a factor of two (Mead, 1989;Andreou et al., 1991). If the distribution is Gaussian as assumed here, these values lie within a range $I_{\mathrm{av}}/9 \approx 1.8$ fA. Fig. 5 indicates that the WSA circuits with $\lambda \leq 0.8$ will perform nearly perfect selection even in the presence of the device mismatches.

5. Concluding remark

We have proposed a MOS circuit representing a Lotka–Volterra competitive neural network and showed its characteristics. The influences of the device mismatches were investigated by circuit simulations, varying the magnitudes of the deviation in the zero-bias current. With the proposed circuits, a large number of unit cells can be integrated on a chip since (i) the complexity of connections is reduced to $O(N)$ by introducing a single inhibitory cell; (ii) the quadratic interaction terms from the original LV neural network were removed by adopting an exponential transfer characteristics for excitatory neuron units, which makes the circuit organization extremely simple; (iii) the electric power dissipation from the circuit is expected to be very small owing to the subthreshold operation of the MOS transistors.

Encouraged by the results of the present simulations, the LV integrated circuit was recently fabricated in Toyohashi University of Technology. The experimental results showed that the circuit does exhibit reliability in WSA solutions (Asai et al., 1997).

References

Andreou, G. A., Boahen, A. K., Pouliquen, O. P., Pavasovic, A., Jenkins, R. E., & Strohbehn, K. (1991). Current-mode subthreshold MOS circuits for analog VLSI neural systems. *IEEE Trans. Neural Networks, 2,* 205–213.

Asai, T., Ohtani, M., & Yonezu, H. (1997). Analog integrated circuits for the Lotka–Volterra competitive neural networks with a winners-share-all solution. In: Proc. Of the 6th. International Conference on Microelectronics for Neural Networks, Evolutionary and Fuzzy Systems (pp. 91–98).

Cohen, A. M., & Grossberg, S. (1983). Absolute stability of global pattern formation and parallel memory storage by competitive neural networks. *IEEE Trans. Systems Man and Cybern., SMC-13,* 815–826.

Fukai, T., & Tanaka, S. (1997). A simple neural network exhibiting selective activation of neuronal ensembles: from winner-take-all to winners-share-all. *Neural Compuration, 9,* 77–97.

Kaski, S., & Kohonen, T. (1994). Winner-take-all networks for physiological models of competitive learning. *Neural Networks*, *7*, 973–984.

Lakshmikumar, R. K., Hadaway, A. R., & Copeland, A. M. (1986). Characterization and modeling of mismatch in MOS transistors for precision analog design. *IEEE J. Solid-State Circuits*, *SC-21*, 1057–1066.

Majani, E., Erlanson, R., & Abu-Mostafa, Y. (1989). On the K-winners-take-all network. *Advances in Neural Information Processing Systems*, I. p. 634–641.

Mead, C. (1989). Analog VLSI and Neural Systems. New York: Addison Wesley.

Pavasovic, A., Anderou, G. A., & Westgate, R. C. (1994). Characterization of subthreshold MOS mismatch in transistors for VLSI systems. *J. Analog Integrated Circuits and Signal Processing*, *6*, 75–85.

Pelgrom, M. J. M., Duinmaijer, J. C. A., & Welbers, G. P. A. (1989). Matching properties of MOS transistors. *IEEE J. Solid-State Circuits*, *24*, 1433–1440.

Taylor, G. J., & Alavi, N. F. (1995). A global competitive neural network. *Biol. Cybern.*, *72*, 233–248.

Wolfe, J. W., Mathis, D., Anderson, C., Rothman, J., Gottler, M., Brady, G., Walker, R., Duane, G., & Alaghband, G. (1991). K-winner networks. *IEEE Trans. Neural Networks*, *2*, 310–315.

Yuille, L. A., & Grzywacz, M. N. (1989). A winner-take-all mechanism based on presynaptic inhibition feedback. *Neural Computation*, *1*, 334–347.